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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,737	11/20/2003	Huilong Zhu	YOR920030479US1	8704

33233 7590 11/21/2005

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/717,737	ZHU ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,5-13,16,18-25 and 48-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,5-13,16,18-25 and 48-58* is/are rejected.

7)☒ Claim(s) *5-7,16 and 48-51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Applicants' amendment filed September 21, 2005.

Claim Objections

Claims 5-7, 16, 49, 51 are objected to because of the following informalities: **device** should have been between "**said**" and "**gate**" in line 2 of claim 5, line 2 of claim 6, line 1 of claim 7, line 2 of claim 16 last line of claim 49 on page 5, and line 1 of claim 51.

Claims 49-50 are objected to because of the following informalities: **side** should have been between "**opposite**" and "**of**" in line 4 of claim 49 on page 5, and line 7 of claim 50.

Claim 50 is objected to because of the following informalities: **"of"** should have been **in** in line 9.

Claims 48-50 are objected to because of the following informalities: **a** should have been before "**back**" in line 7, line 4 on page 5 and line 7, respectively.

Claims 48-50 are objected to because of the following informalities: **a** should have been before "**device**" in line 5, line 2 on page 5 and line 5, respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3, 5-9, 48 and 50-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sin et al. (5,982,004) in view of Chan et al. (US 6,580,132 B1).

In regard to claim 48, Sin et al. teach a field effect transistor (FET) comprising: a fin formed on a dielectric surface; a device gate (FLOATING GATE) along one side of the fin; a back bias gate (BACK-PLATE) along an opposite side of the fin; device gate dielectric along one first side between the device gate (FLOATING GATE) and the fin; and back bias gate dielectric (TUNNEL OXIDE) along the opposite side between the back bias gate (BACK-PLATE) and the fin, wherein the back bias gate dielectric differs from the device gate dielectric (TUNNEL OXIDE) in material (Figure 6, columns 6-7, lines 57-67 and 1-14, respectively).

In regard to claims 2-3, Sin et al. teach a silicon semiconductor fin (column 4, line 25).

In regard to claim 5, Sin et al. teach the back bias gate dielectric being thicker than the gate dielectric (Figure 6).

In regard to claim 6, Sin et al. teach each of the back bias gate dielectric and the gate dielectric being an oxide (column 4, lines 18-44).

In regard to claims 8 and 52, Sin et al. teach the dielectric surface being an oxide layer (column 4, lines 18-44).

In regard to claims 9 and 53, Sin et al. teach the oxide layer being a buried oxide layer (Figure 6, column 4, lines 18-44).

In regard to claim 50, Sin et al. teach an integrated circuit (IC) on a semiconductor on insulator (SOI) chip, the IC including a plurality of field effect transistors (FETs) disposed on an insulating layer, each of the FETs comprising: a semiconductor fin formed on an insulating layer; device gat dielectric (TUNNEL OXIDE) along a first side of the semiconductor fin; a device gate (FLOATING GATE) along the device gate dielectric (TUNNEL OXIDE); back bias gate dielectric along an opposite of the semiconductor fin; a back bias gate (BACK-PLATE) along the back bias gate dielectric, wherein the back bias gate dielectric differs from the device gate dielectric of material, wherein one of the device gate dielectric and the back bias gate dielectric are a layered dielectric comprising at least 2 dielectric material layers (Figure 6, columns 6-7, lines 57-67 and 1-14, respectively).

However, Sin et al. fail to teach one of the device gate dielectric and the back bias gate dielectric are a layered dielectric comprising at least 2 dielectric material layers.

Chan et al. teach one of a device gate dielectric 22 and a back bias gate dielectric 68 being a layered dielectric comprising at least 2 dielectric material layers (Figure 2B, columns 4, 8 and 10, lines 65-67, 45-48 and 44-44, respectively).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the field effect transistor (FET) structure as taught by Sin et al. with the field effect transistor (FET) having one of the device gate

dielectric and the back bias gate dielectric are a layered dielectric comprising at least 2 dielectric material layers as taught by Chan et al. to reduce threshold voltage roll-off (column 2, lines 58-60).

In regard to claims 7 and 51, Chan et al. teach the device gate 20 and the back bias gate 70 being a metal (column 10, lines 25-30).

Claims 11 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sin et al. (5,982,004) and Chan et al. (US 6,580,132 B1) as applied to claims 2-3, 5-9, 48 and 50-53 above, and further in view of Fried et al. (US 2003/0178670 A1).

Sin et al. and Chan et al. teach all mentioned in the rejection above.

However, Sin et al. and Chan et al. fail to teach a dielectric pillar above a semiconductor silicon fin.

Fried et al. teach a dielectric pillar 102 above a semiconductor silicon fin 100 (Figure 11, page 3, paragraphs [0030] and [0038]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the field effect transistor (FET) structure as taught by Sin et al. and the field effect transistor (FET) having one of the device gate dielectric and the back bias gate dielectric are a layered dielectric comprising at least 2 dielectric material layers as taught by Chan et al. with the field effect transistor having a dielectric pillar above a semiconductor silicon fin as taught by Fried et al. to allow horizontal current flow (abstract).

Claims 10, 12-13 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sin et al. (5,982,004) and Chan et al. (US 6,580,132 B1) as applied to claims 2-3, 5-9, 48 and 50-53 above, and further in view of Mathew et al. (US 2003/0151077 A1).

Sin et al. and Chan et al. teach all mentioned in the rejection above.

However, Sin et al. and Chan et al. fail to teach a dielectric pillar being a nitride pillar, and the nitride pillar forming a cap between a device gate and a back bias gate.

In regard to claim 10, Mathew et al. teach an oxide layer 14 disposed on a nitride layer 12 (Figure 15, page 1, paragraph [0016]).

In regard to claims 12-13 and 54, Mathew et al. teach a dielectric pillar 22 being a nitride pillar, and the nitride pillar forming a cap between a gates 62' and 64' (Figure 15, pages 2-3, paragraphs [0017] and [0031], respectively).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the field effect transistor (FET) structure as taught by Sin et al. and the field effect transistor (FET) having one of the device gate dielectric and the back bias gate dielectric are a layered dielectric comprising at least 2 dielectric material layers as taught by Chan et al. with the field effect transistor having a dielectric pillar being a nitride pillar, and the nitride pillar forming a cap between a device gate and a back bias gate as taught by Mathew et al. to provide a device that is able to be made with reduced dimensions and still function at the required specifications (page 1, paragraph [0002]).

Claims 56-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sin et al. (5,982,004), Chan et al. (US 6,580,132 B1) and Fried et al. (US 2003/0178670 A1) as applied to claims 11 and 55 above, and further in view of Mathew et al. (US 2003/0151077 A1).

Sin et al., Chan et al. and Fried et al. teach all mentioned in the rejection above.

In regard to claim 58, Sin et al. further teach the semiconductor being silicon (Figure 6).

However, Sin et al., Chan et al. and Fried et al. fail to teach a dielectric pillar being a nitride pillar, and the nitride pillar forming a cap between a device gate and a back bias gate.

In regard to claims 56-57, Mathew et al. teach a dielectric pillar 22 being a nitride pillar, and the nitride pillar forming a cap between a gates 62' and 64' (Figure 15, pages 2-3, paragraphs [0017] and [0031], respectively).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the field effect transistor (FET) structure as taught by Sin et al., the field effect transistor (FET) having one of the device gate dielectric and the back bias gate dielectric are a layered dielectric comprising at least 2 dielectric material layers as taught by Chan et al. and the field effect transistor having a dielectric pillar above a semiconductor silicon fin as taught by Fried et al. with the field effect transistor having a dielectric pillar being a nitride pillar, and the nitride pillar forming a cap between a device gate and a back bias gate as taught by Mathew et al. to

provide a device that is able to be made with reduced dimensions and still function at the required specifications (page 1, paragraph [0002]).

Claims 16, 18-20 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sin et al. (5,982,004) and Chan et al. (US 6,580,132 B1) in view of Chan et al. (US 6,946,696 B2).

Sin et al. and Chan et al. (US 6,580,132 B1) teach all mentioned in the rejection above.

In regard to claim 16, Sin et al. teach each of the back bias gate dielectric and the gate dielectric being an oxide (column 4, lines 18-44).

In regard to claim 19, Sin et al. teach the dielectric surface being an oxide layer (column 4, lines 18-44).

In regard to claim 20, Sin et al. teach the oxide layer being a buried oxide layer (Figure 6, column 4, lines 18-44).

In regard to claim 49, Sin et al. teach an integrated circuit (IC) on a semiconductor on insulator (SOI) chip, the IC including a plurality of field effect transistors (FETs) disposed on an insulating layer, each of the FETs comprising: a semiconductor fin formed on an insulating layer; device gat dielectric (TUNNEL OXIDE) along a first side of the semiconductor fin; a device gate (FLOATING GATE) along the device gate dielectric (TUNNEL OXIDE); back bias gate dielectric along an opposite of the semiconductor fin; a back bias gate (BACK-PLATE) along the back bias gate dielectric (Figure 6, columns 6-7, lines 57-67 and 1-14, respectively).

In regard to claim 18, Chan et al. (US 6,580,132 B1) teach the device gate 20 and the back bias gate 70 being a metal (column 10, lines 25-30).

However, Sin et al. and Chan et al. (US 6,580,132 B1) fail to teach the back bias gate dielectric being five times (5X) thicker than the device gate dielectric.

Chan et al. (US 6,946,696 B2) teach the back bias gate dielectric being several times thicker than the device gate dielectric (column 2, lines 13-23).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the field effect transistor (FET) structure as taught by Sin et al. and the field effect transistor (FET) having one of the device gate dielectric and the back bias gate dielectric are a layered dielectric comprising at least 2 dielectric material layers as taught by Chan et al. (US 6,580,132 B1) with the field effect transistor (FET) having the back bias gate dielectric being several times thicker than the device gate dielectric as taught by Chan et al. (US 6,946,696 B2) to reduce parasitic capacitance (column 2, lines 13-23).

Claims 21, 23-24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sin et al. (5,982,004), Chan et al. (US 6,580,132 B1) and Chan et al. (US 6,946,696 B2) as applied to claims 16, 18-20 and 49 above, and further in view of Mathew et al. (US 2003/0151077 A1).

Sin et al., Chan et al. (US 6,580,132 B1) and Chan et al. (US 6,946,696 B2) teach all mentioned in the rejection above.

In regard to claim 25, Sin et al. teach a silicon semiconductor (Figure 6).

However, Sin et al., Chan et al. (US 6,580,132 B1) and Chan et al. (US 6,946,696 B2) fail to teach a dielectric pillar being a nitride pillar, and the nitride pillar forming a cap between a device gate and a back bias gate.

In regard to claim 21, Mathew et al. teach an oxide layer 14 disposed on a nitride layer 12 (Figure 15, page 1, paragraph [0016]).

In regard to claims 23-24, Mathew et al. teach a dielectric pillar 22 being a nitride pillar, and the nitride pillar forming a cap between a gates 62' and 64' (Figure 15, pages 2-3, paragraphs [0017] and [0031], respectively).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the field effect transistor (FET) structure as taught by Sin et al. and the field effect transistor (FET) having one of the device gate dielectric and the back bias gate dielectric are a layered dielectric comprising at least 2 dielectric material layers as taught by Chan et al. (US 6,580,132 B1) and the field effect transistor (FET) having the back bias gate dielectric being several times thicker than the device gate dielectric as taught by Chan et al. (US 6,946,696 B2) with the field effect transistor having a dielectric pillar being a nitride pillar, and the nitride pillar forming a cap between a device gate and a back bias gate as taught by Mathew et al. to provide a device that is able to be made with reduced dimensions and still function at the required specifications (page 1, paragraph [0002]).

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sin et al. (5,982,004), Chan et al. (US 6,580,132 B1) and Chan et al. (US 6,946,696 B2) as

applied to claims 21, 23-24 and 25 above, and further in view of Fried et al. (US 2003/0178670 A1).

Sin et al., Chan et al. (US 6,580,132 B1) and Chan et al. (US 6,946,696 B2) teach all mentioned in the rejection above.

However, Sin et al., Chan et al. (US 6,580,132 B1) and Chan et al. (US 6,946,696 B2) fail to teach a dielectric pillar above a semiconductor silicon fin.

Fried et al. teach a dielectric pillar 102 above a semiconductor silicon fin 100 (Figure 11, page 3, paragraphs [0030] and [0038]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the field effect transistor (FET) structure as taught by Sin et al. and the field effect transistor (FET) having one of the device gate dielectric and the back bias gate dielectric are a layered dielectric comprising at least 2 dielectric material layers as taught by Chan et al. (US 6,580,132 B1) and the field effect transistor (FET) having the back bias gate dielectric being several times thicker than the device gate dielectric as taught by Chan et al. (US 6,946,696 B2) with the field effect transistor having a dielectric pillar above a semiconductor silicon fin as taught by Fried et al. to allow horizontal current flow (abstract).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to FinFETs:

Bryant et al. (US 6,960,806 B2)

Dokumaci et al. (US 2005/0059252 A1)

Forbes et al. (US 2004/0161886 A1)

Tsuji (5,315,143)

Yu (US 6,458,662 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
November 17, 2005